Silicon Integration for Convergence

Sunlin Chou
Senior Vice President
General Manager
Technology and Manufacturing Group

April 2003

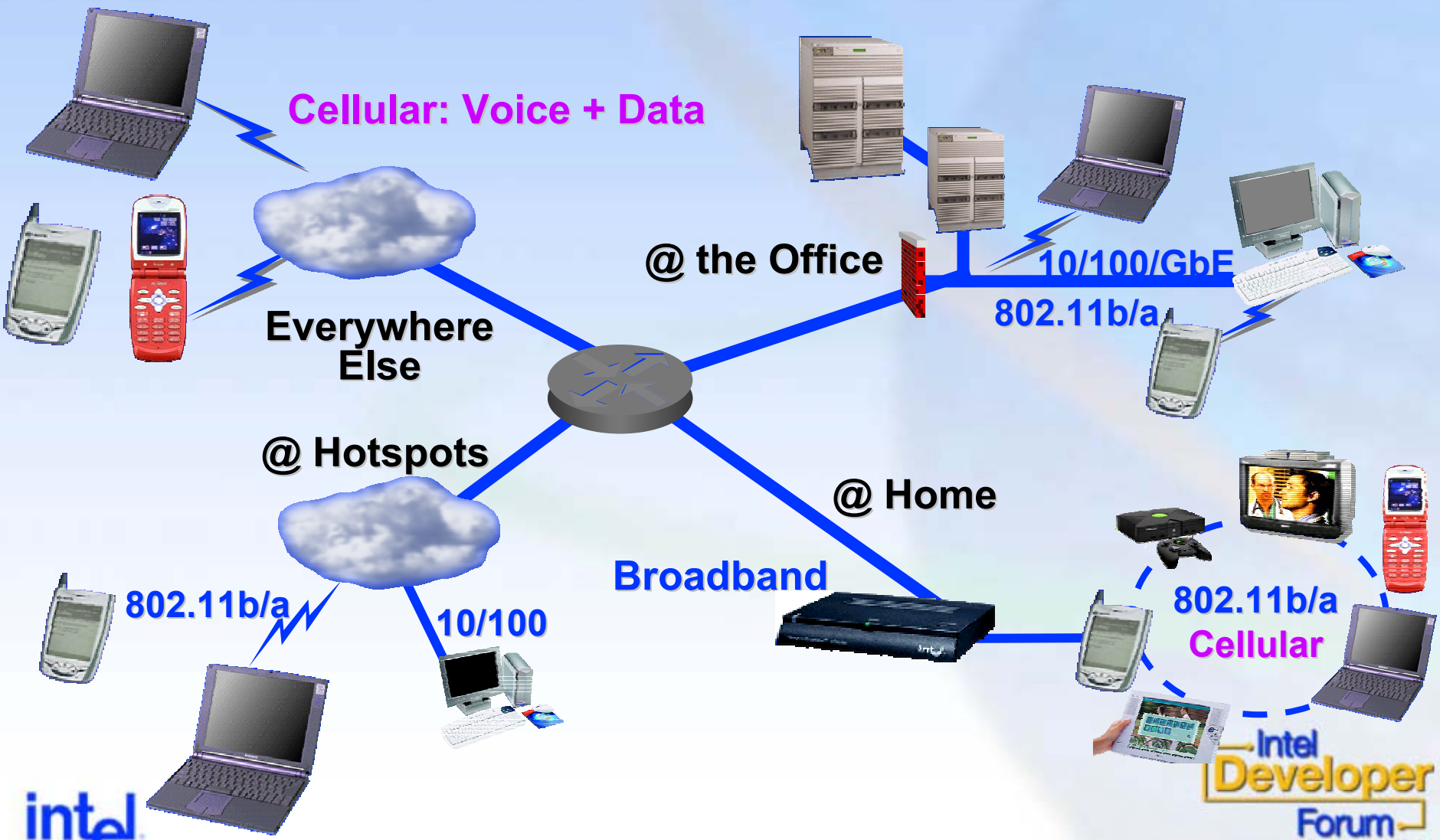
Silicon Integration for Convergence: Three Strategic Combinations

- Computing + Communications
- CMOS Base + Application Specific Modules
- Silicon Technology Base + Nanotechnology

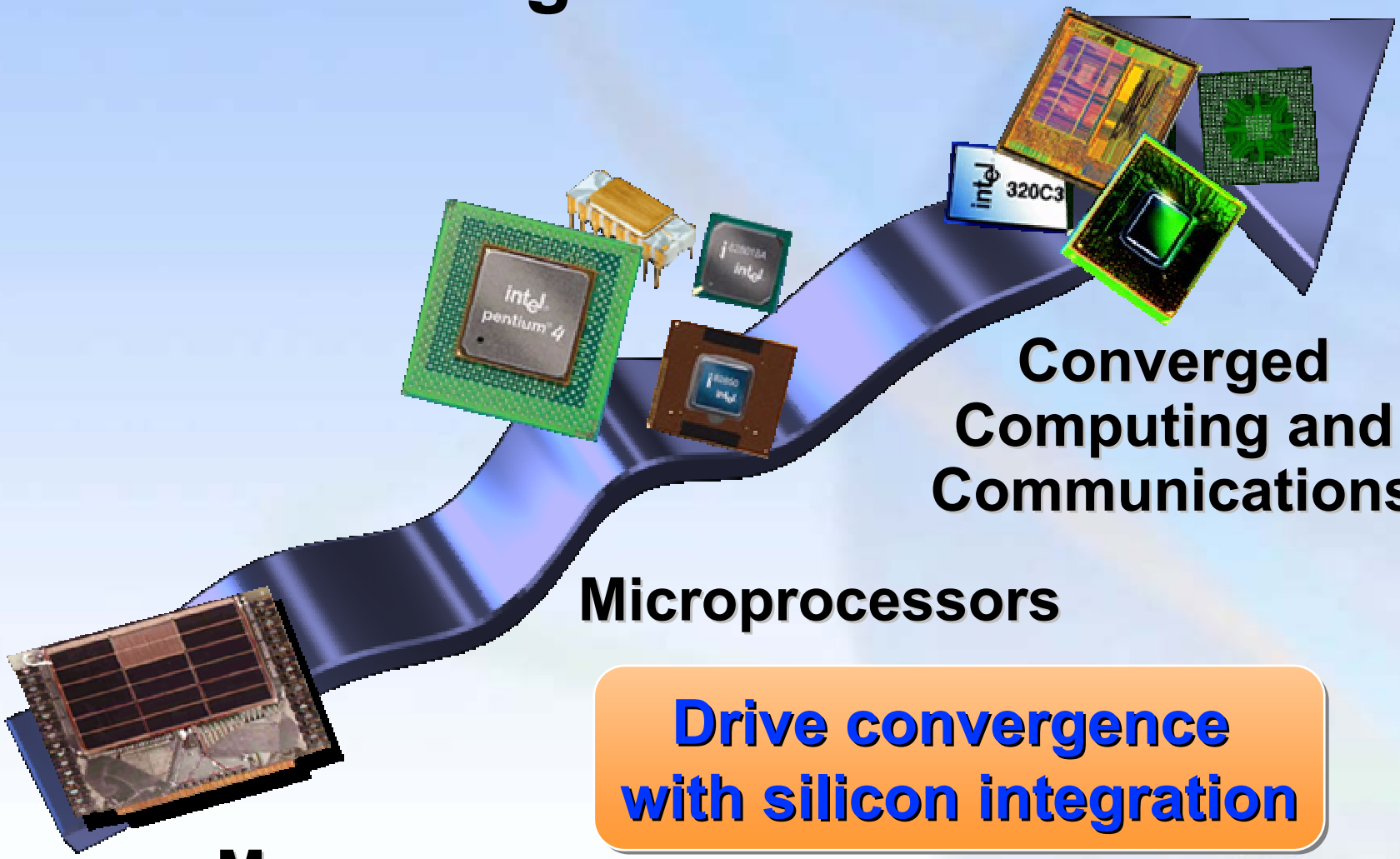
Silicon Integration for Convergence: Three Strategic Combinations

- **Computing + Communications**
- CMOS Base + Application Specific Modules
- Silicon Technology Base + Nanotechnology

Computing + Communications Vision: Data Anytime, Anywhere



Silicon is the Engine



Converged Computing and Communications

Microprocessors

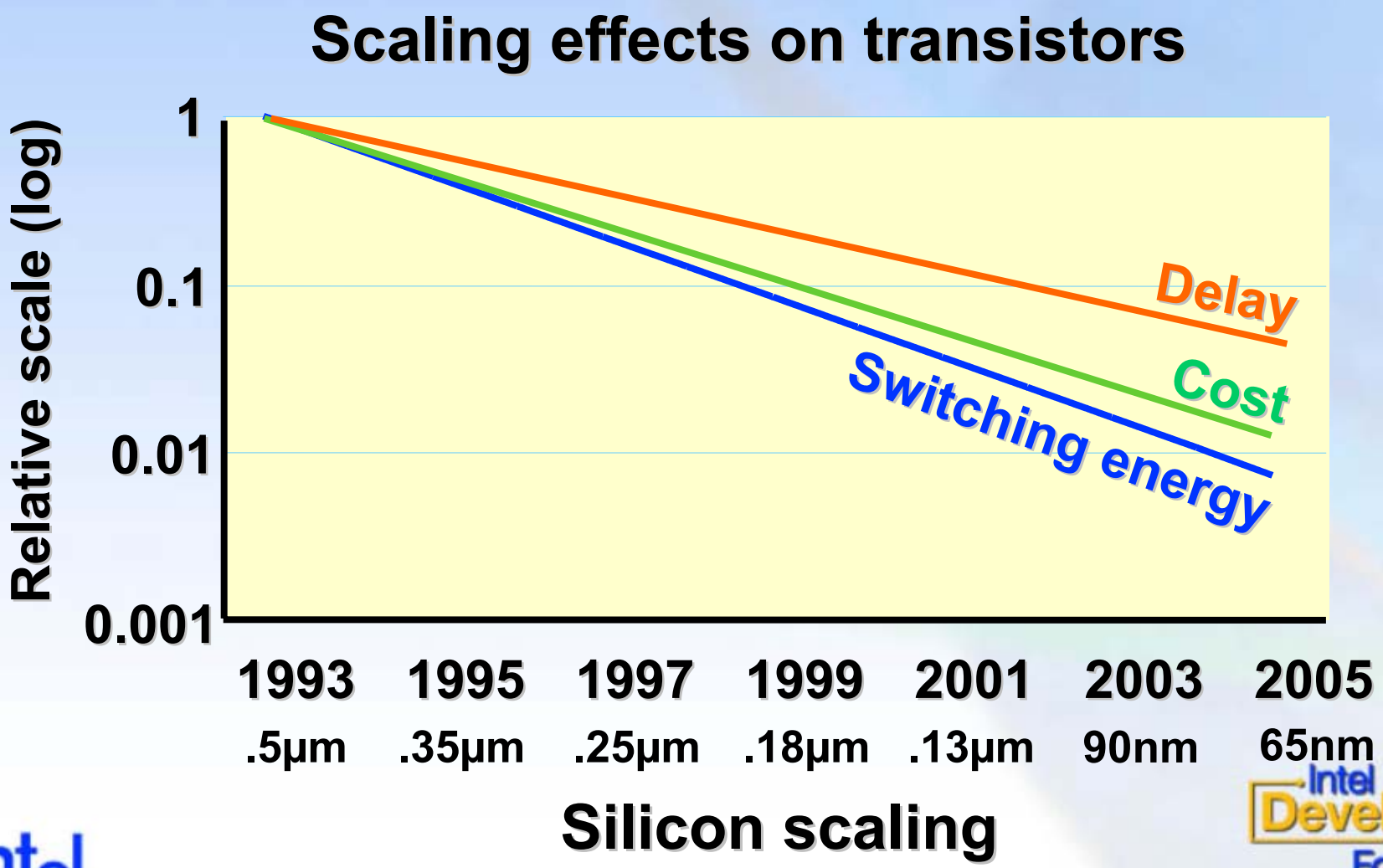
Memory

Drive convergence with silicon integration

intel

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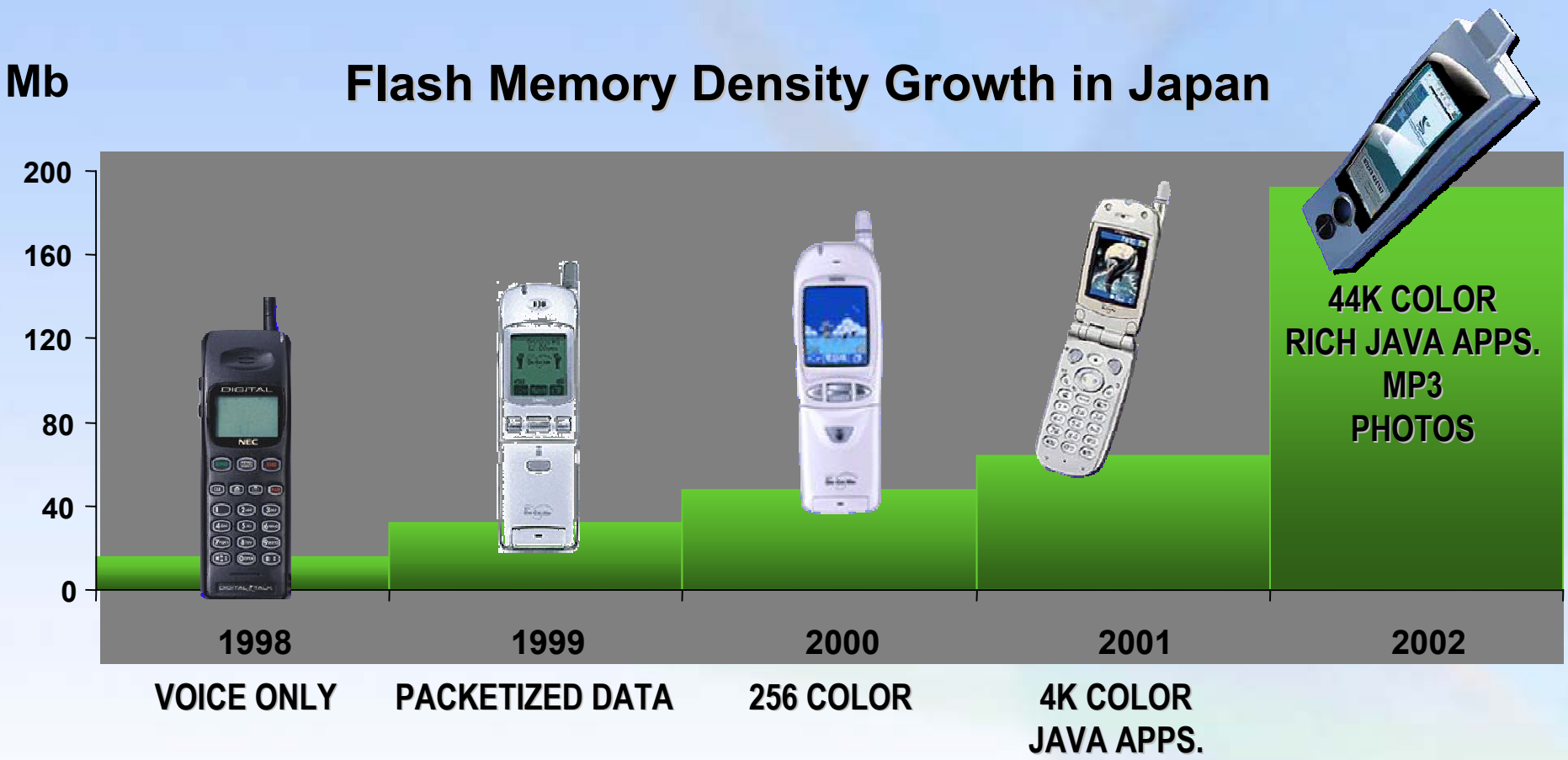
Silicon Scaling and Integration Improve Performance, Power, Cost



Source: Intel

intel
Intel Developer Forum Spring 2003

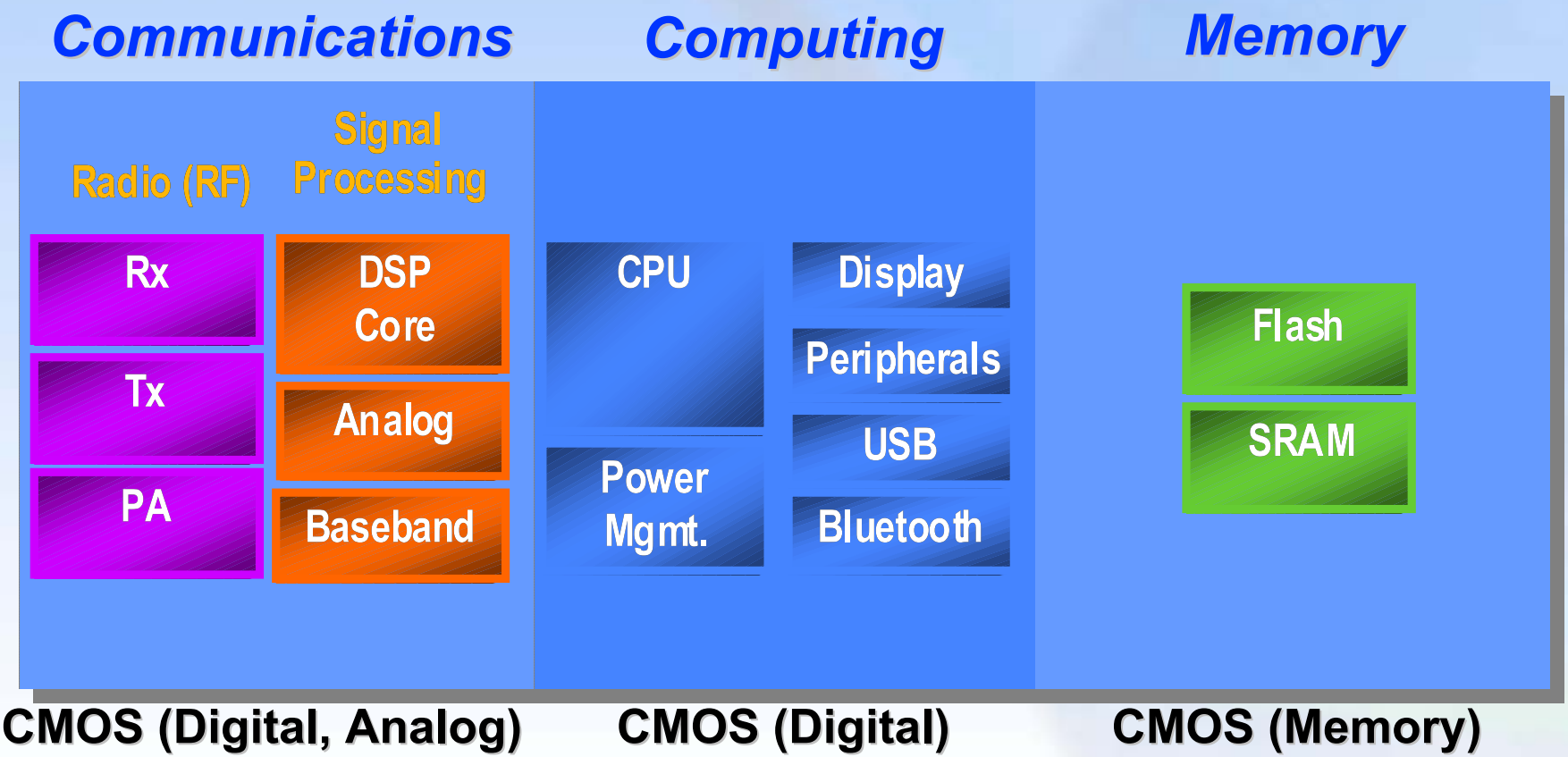
Cell Phones For Voice + Data



Convergence increases silicon usage

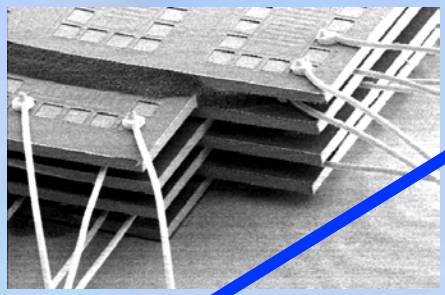
Source: NEC, Intel

Converged Cell Phone Integration Opportunities



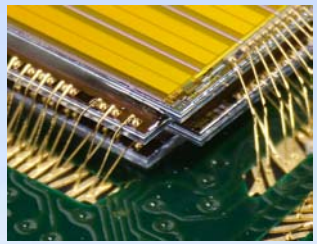
Integration via Packaging

Under Research



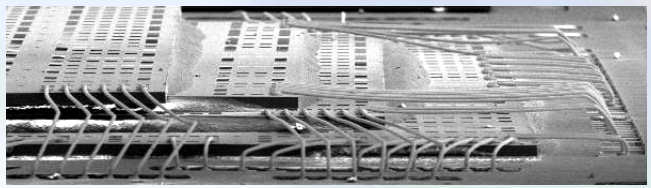
Ultrathin Stacked
Chip Scale Packaging
2003

8 Die Stack
50 µm Die

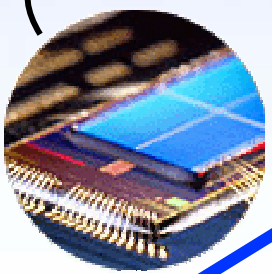


4 to 5 Die
1 to 1.2 mm

75 µm Die Thinness



>150 M Units
Shipped



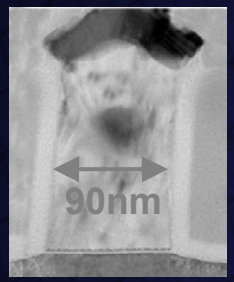
2 to 3 Die
1.2mm

125 - 175 µm Die
Thickness

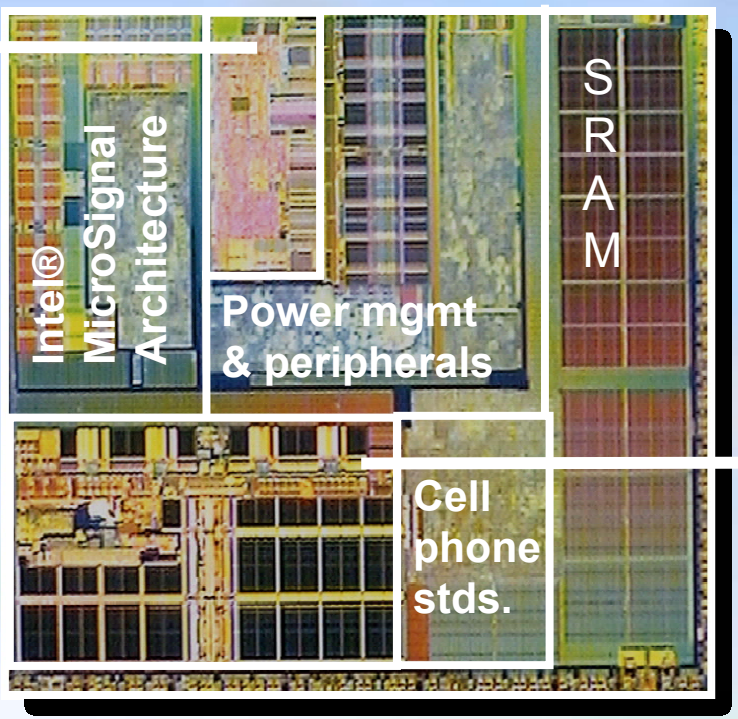
2 Die
1.4mm Package Height

Wireless Internet on a Chip by Flash+Logic Integration

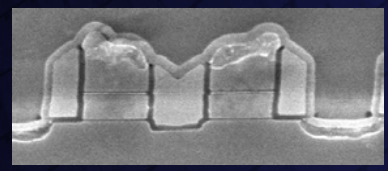
Logic



90nm Transistor Gate on 0.13µm Process



Flash



0.16µm² Flash Cell

PXA800F Cellular Processor

Integration improves density, speed, power consumption

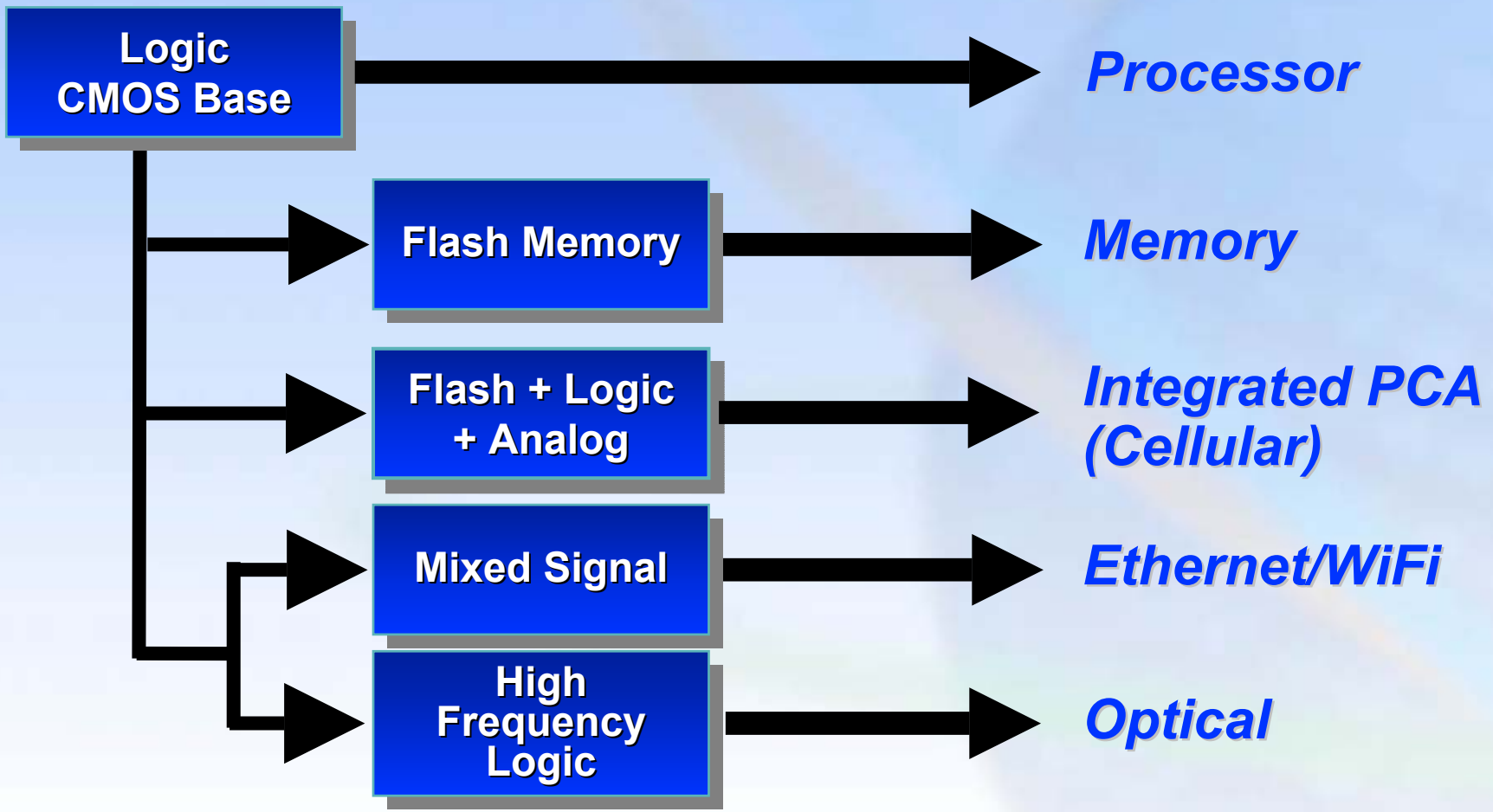
Source: Intel

intel
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Silicon Integration for Convergence: Three Strategic Combinations

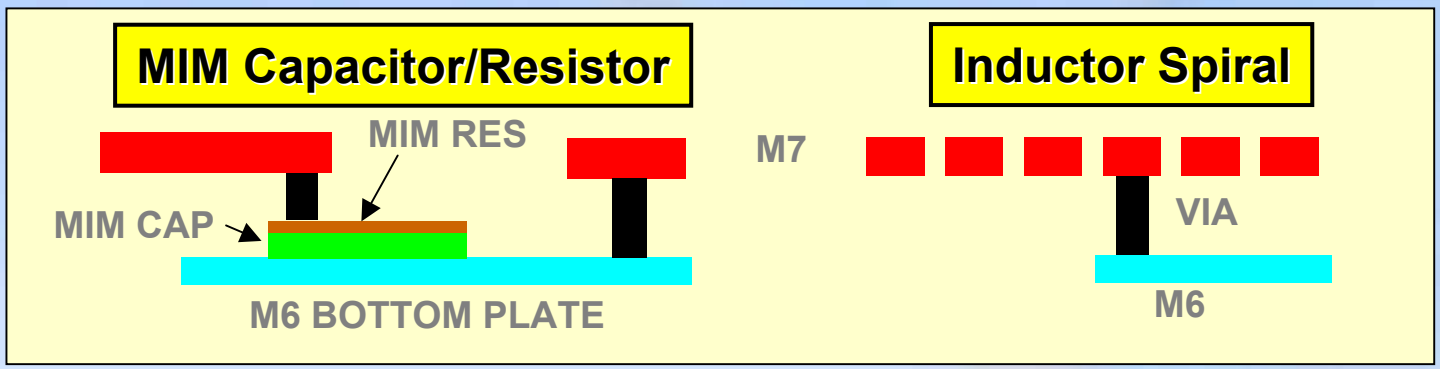
- Computing + Communications
- **CMOS Base + Application Specific Modules**
- Silicon Technology Base + Nanotechnology

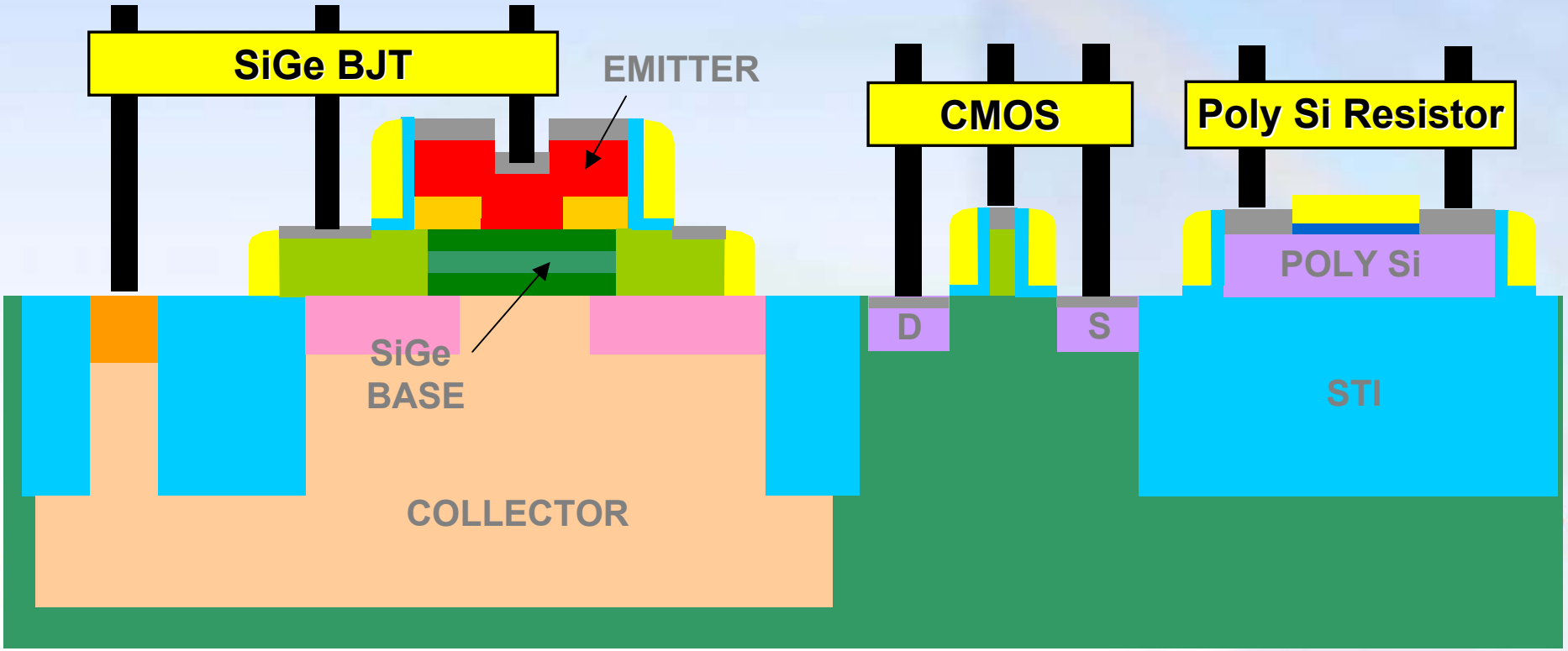
Intel's Technologies for Convergence: CMOS Base + Apps-Specific Modules



Economy of scale (shared base)
+ application-specific optimization

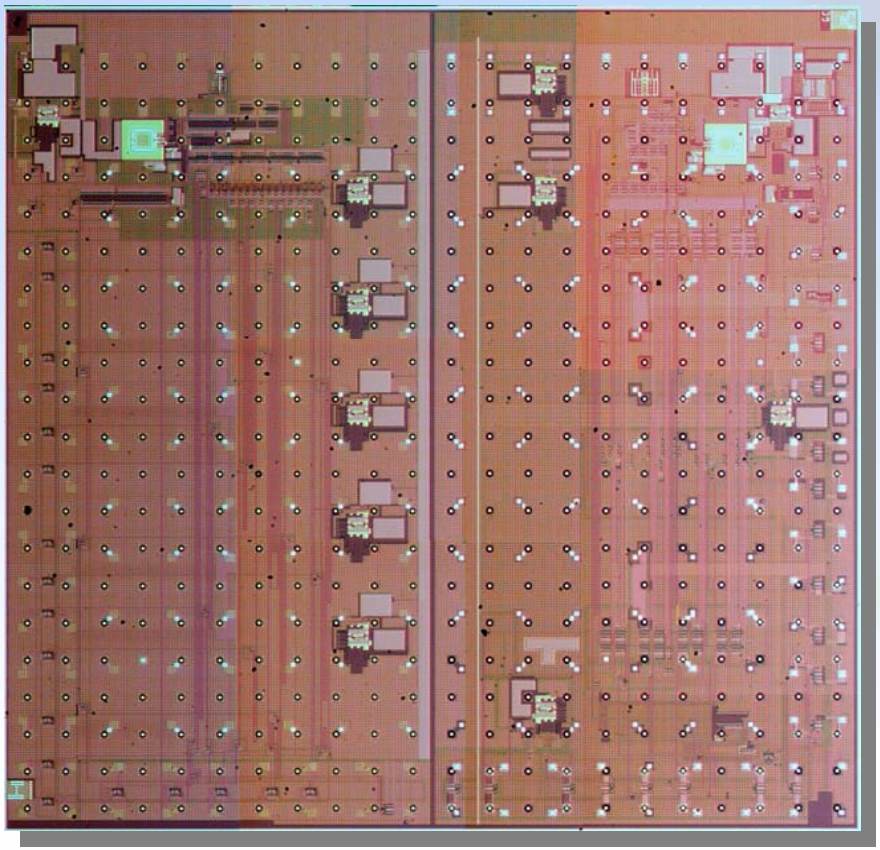
Process Modules Available for Ethernet/WiFi and Optical Comm

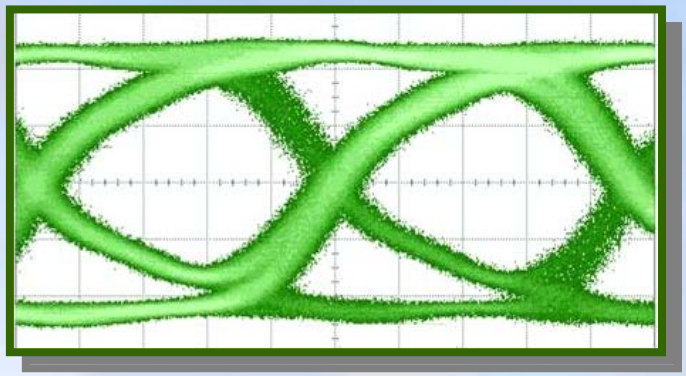




10Gb/s SONET Transceiver on 90nm Technology

RX TX





Output @ 10.66Gb/s

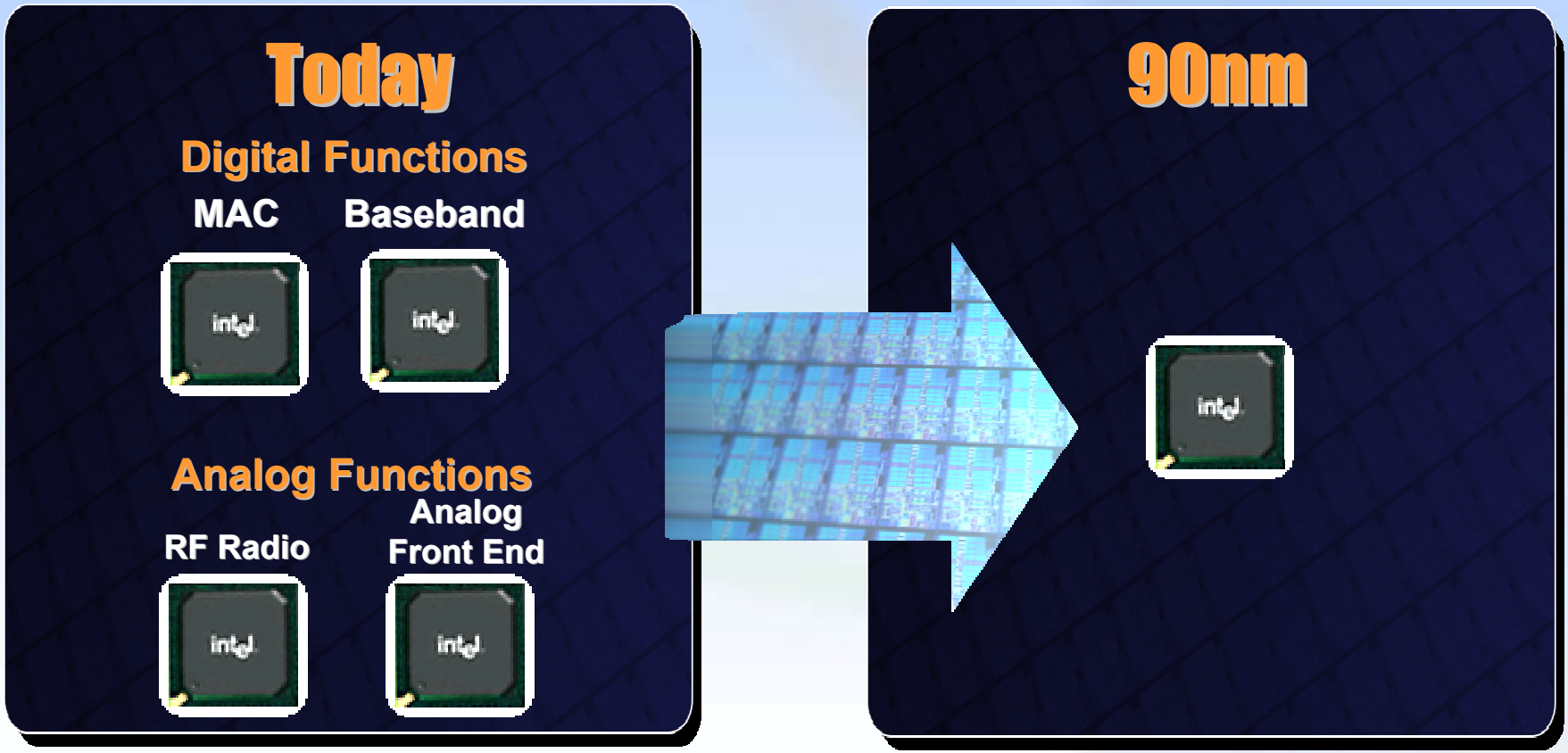
Single chip CMOS

Precision passives (R, L, C)

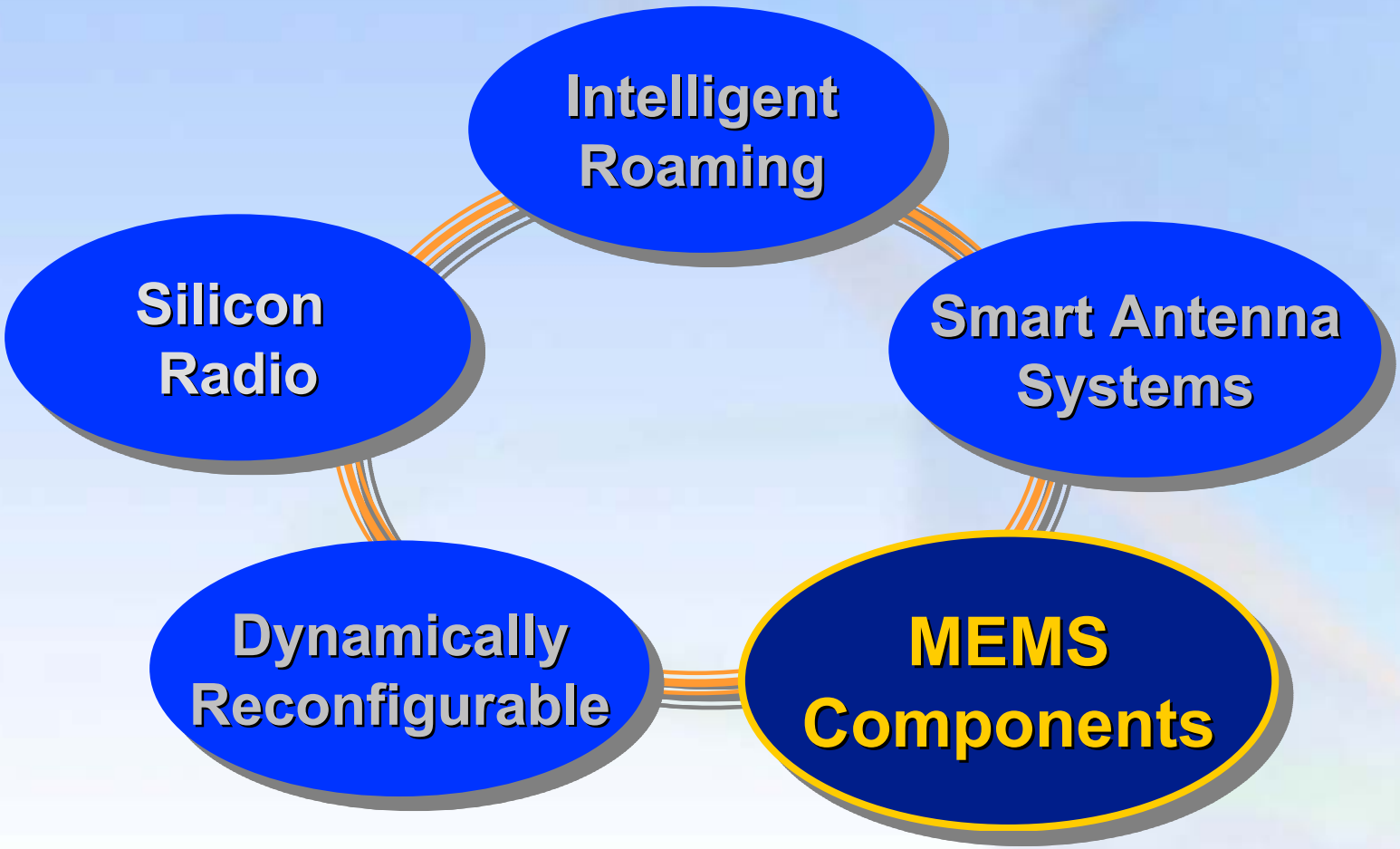
Source: Intel

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802.11 (WiFi) Integration Improves Cost and Power

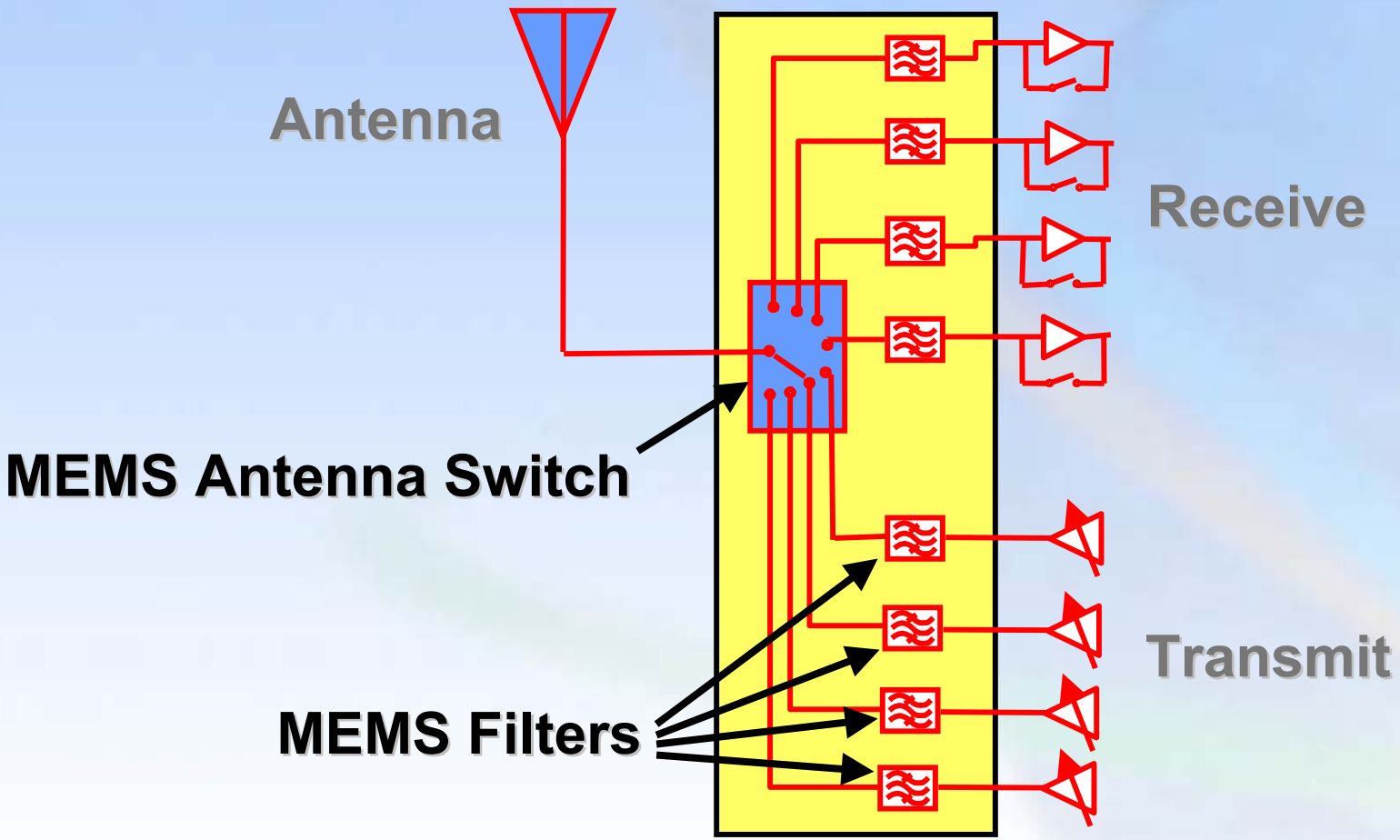


Radio Research at Intel



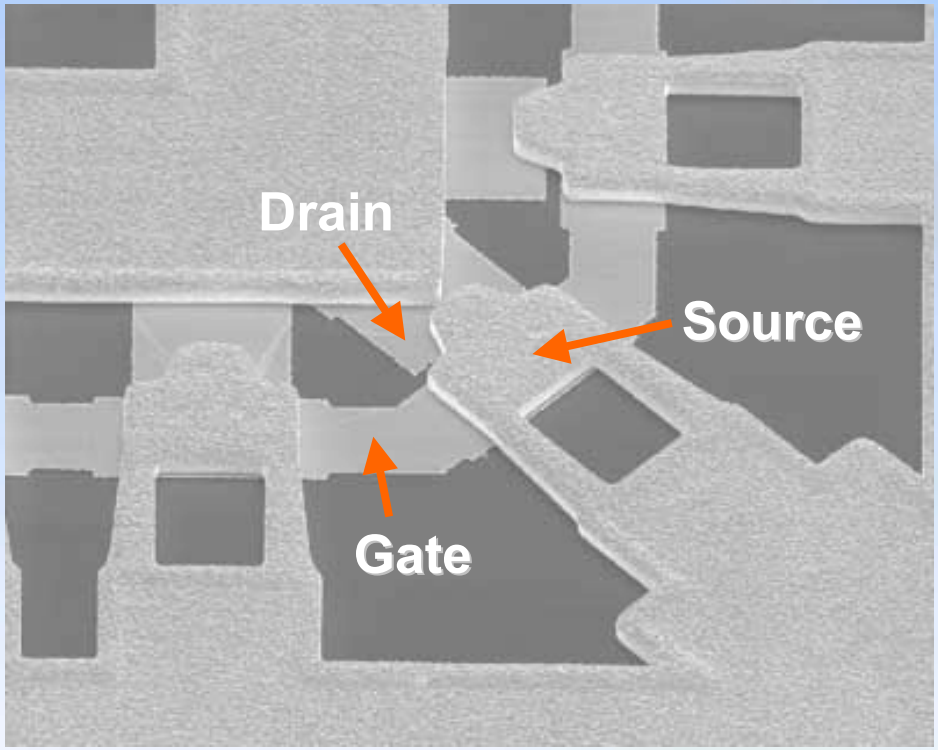
MEMS: Micro Electro Mechanical Systems

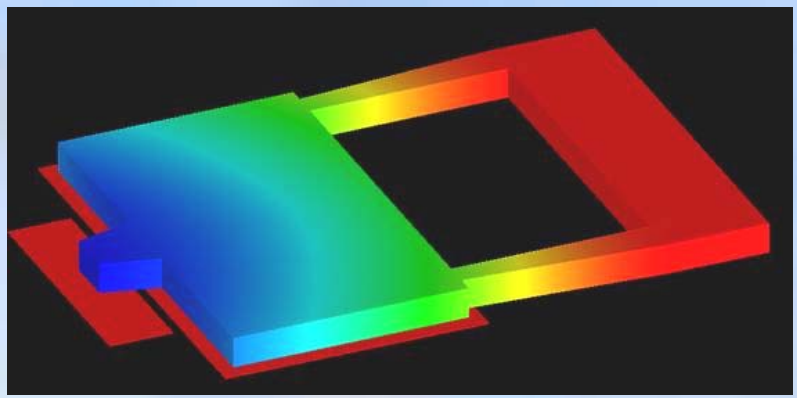
MEMS Antenna Switches and Filters for Multi Band Radios



MEMS benefits: Low insertion loss + component integration

Integrated MEMS RF Switches





Switch design

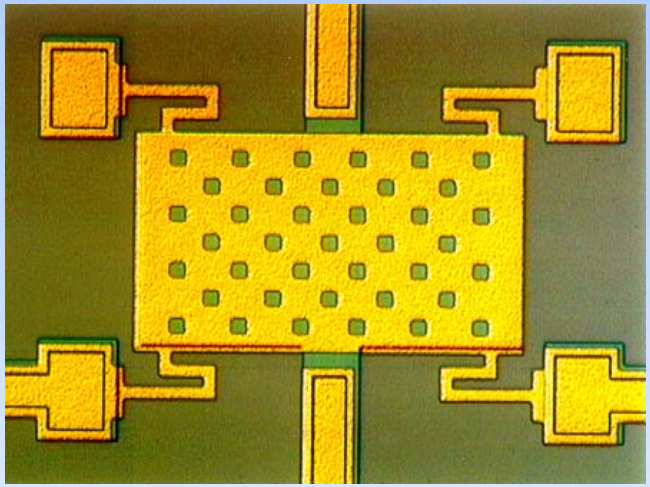
Multiple gold RF switches integrated into one silicon MEMS chip

Fabricated using silicon processing technology

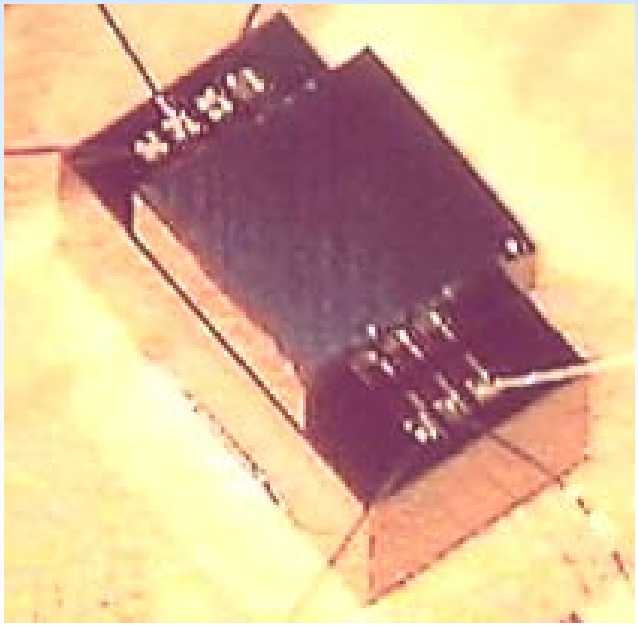
Source: Intel

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MEMS Integrated with CMOS



MEMS Varactor



MEMS Varactor flip chip bonded to a CMOS VCO

Source: Intel

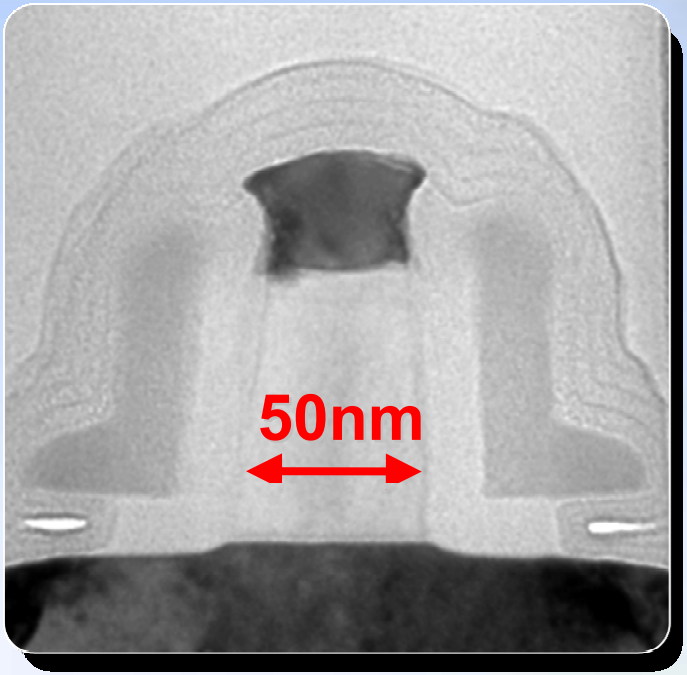
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Silicon Integration for Convergence: Three Strategic Combinations

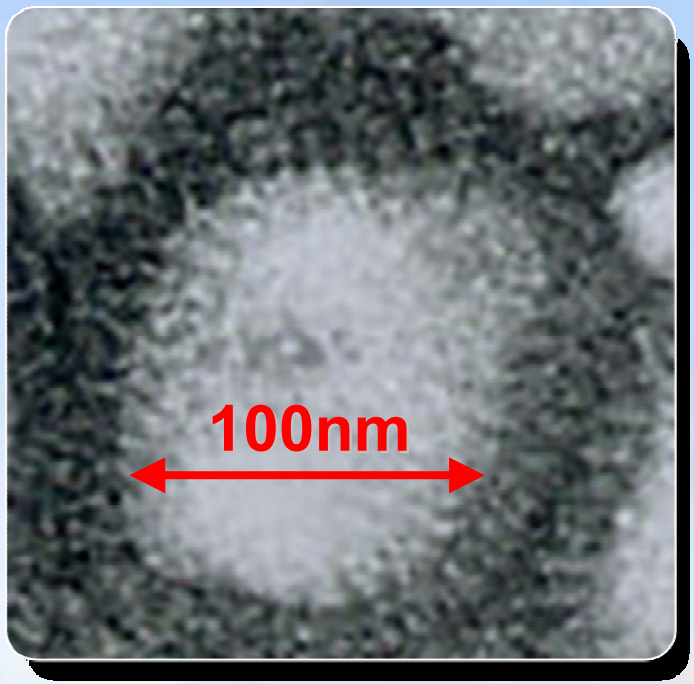
- Computing + Communications
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- **Silicon Technology Base + Nanotechnology**

Silicon Devices Shrink to Virus Size..



Transistor for 90nm Process

Source: Intel

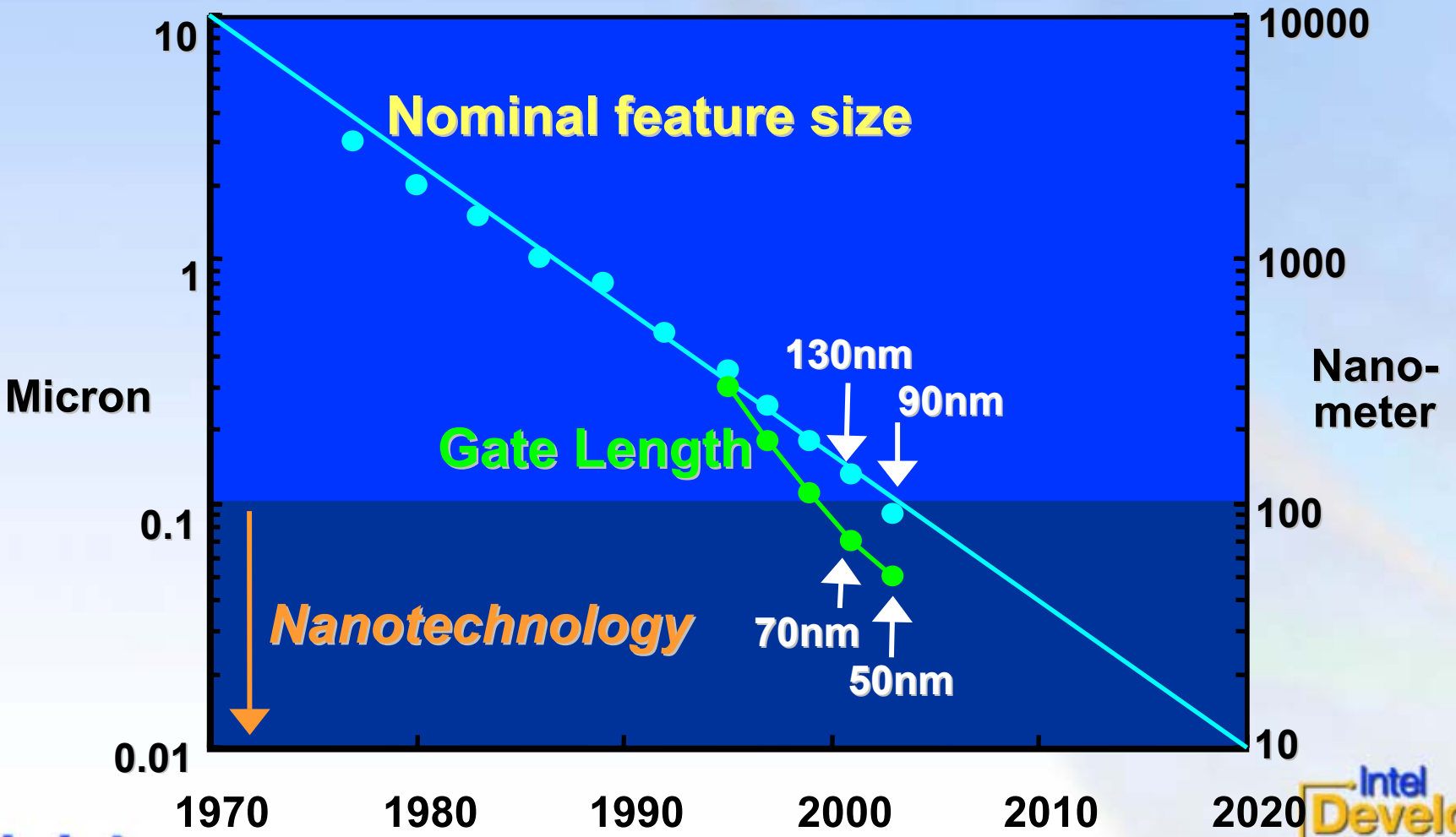


Influenza virus

Source: CDC

..and Nanotechnology Scale

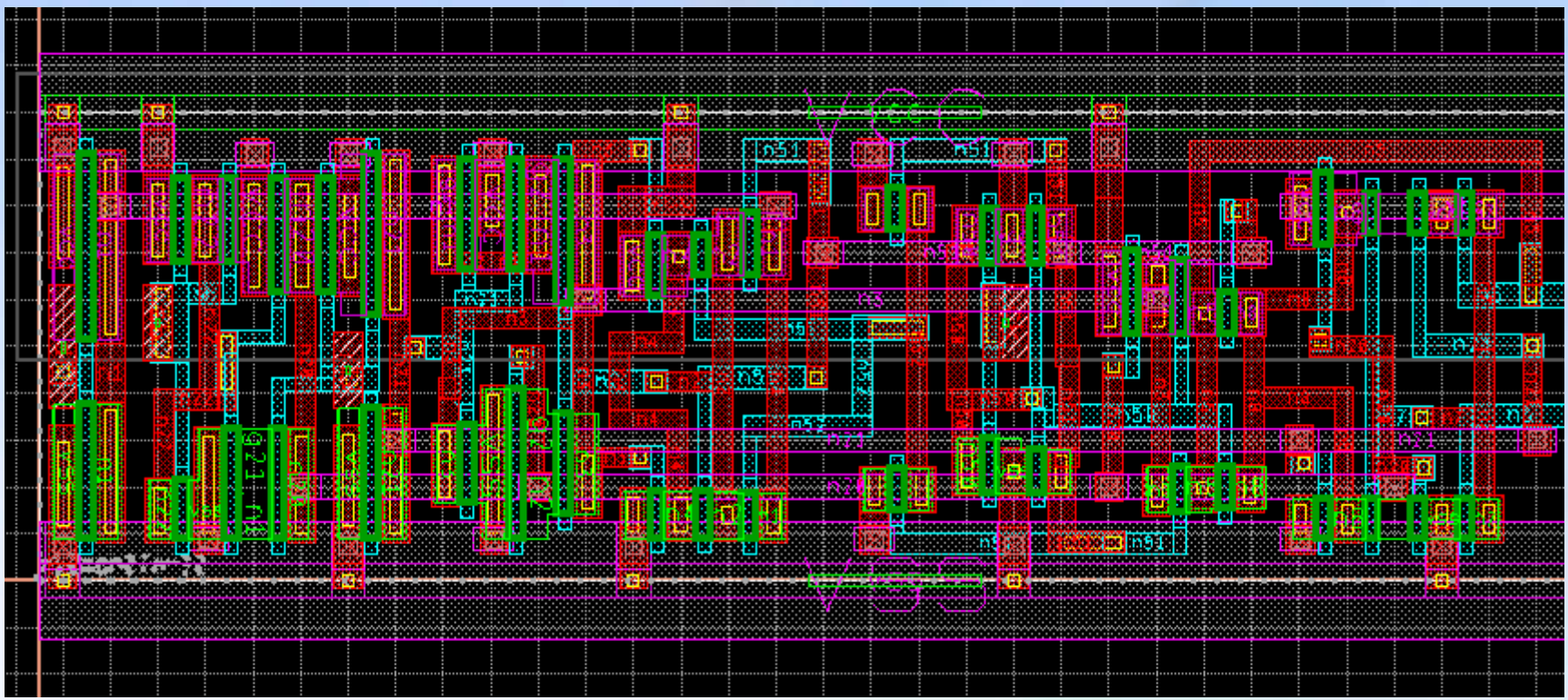
Intel in Production with Nanotechnology (< 100nm)



Source: Intel

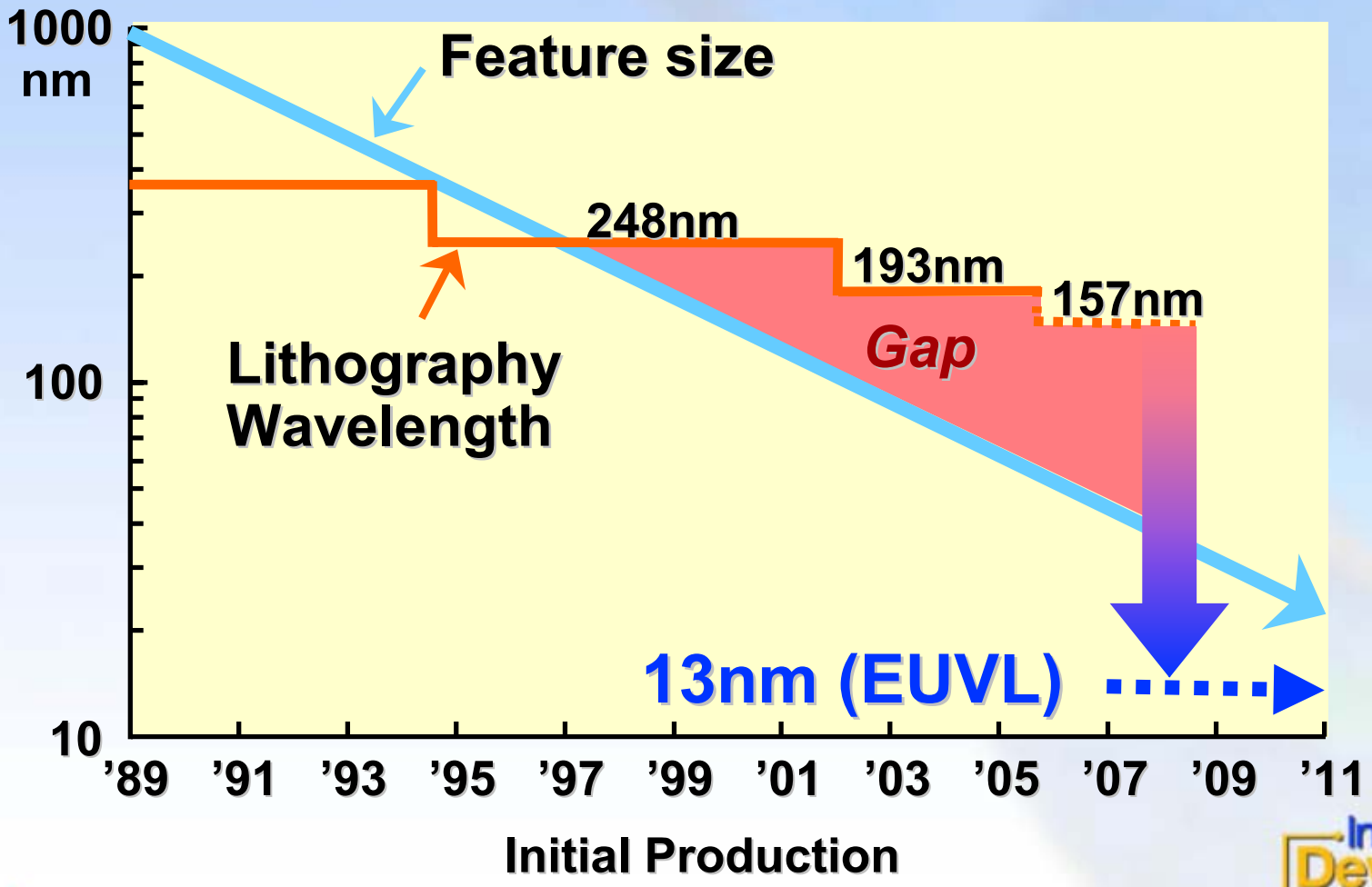
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Lithography is the Designer's "Brush"



Lithography is indispensable for defining locations/configurations of circuit elements/functions

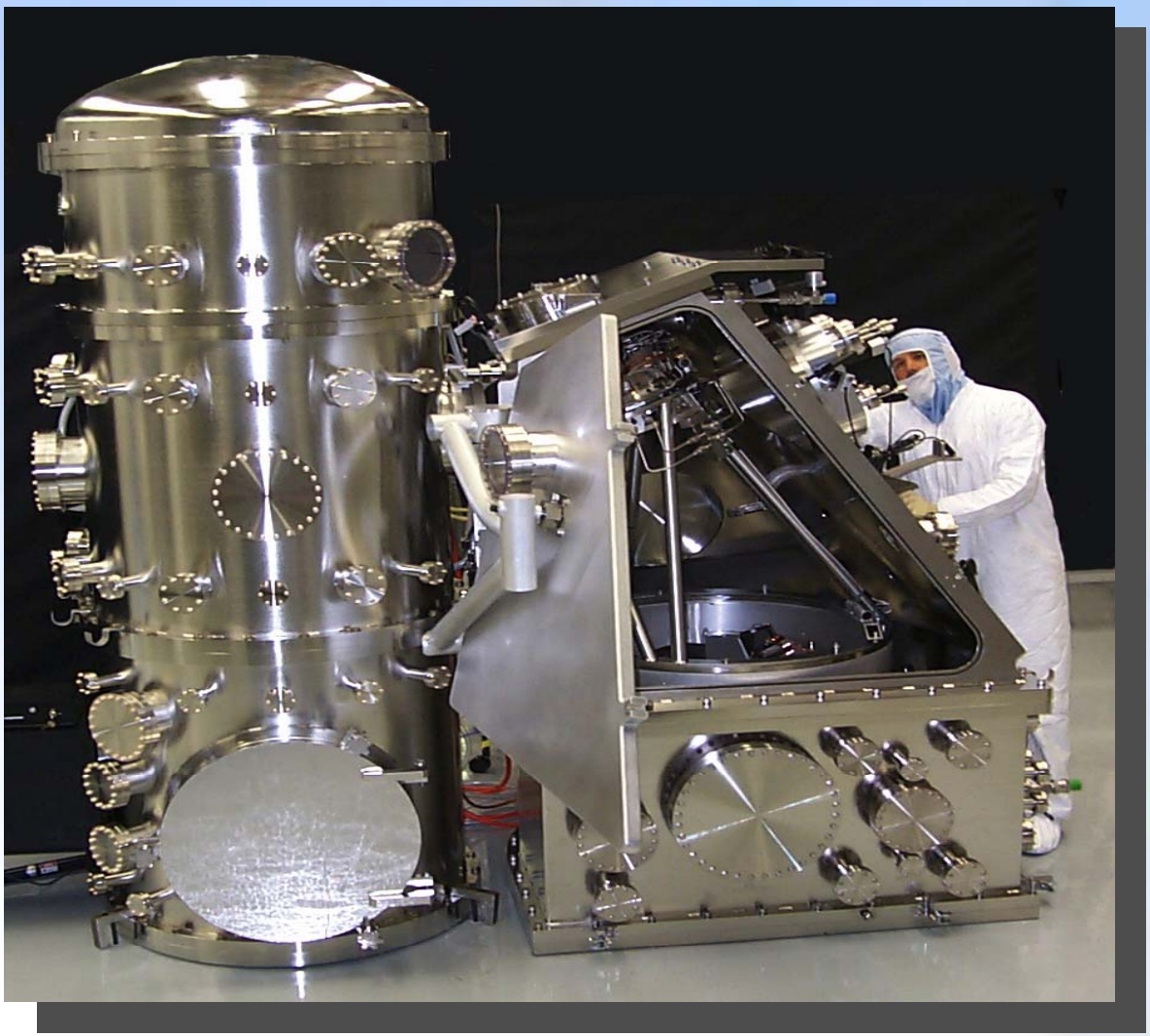
Lithography Gap to Close with EUVL (Extreme Ultra Violet Lithography)



Source: Intel

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EUV LLC Consortium Demonstrates EUVL with Prototype Exposure Tool

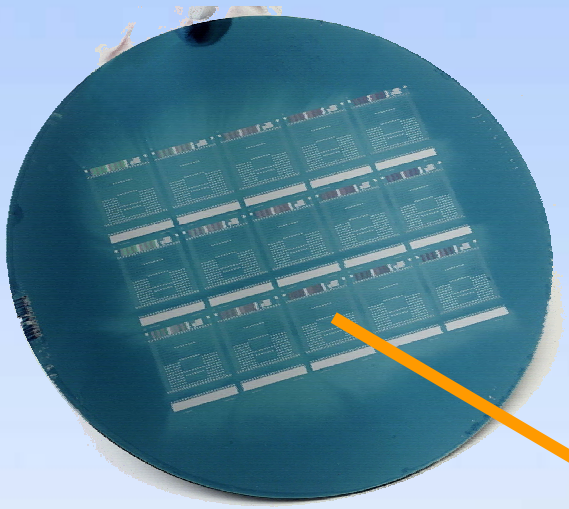


Source: Sandia

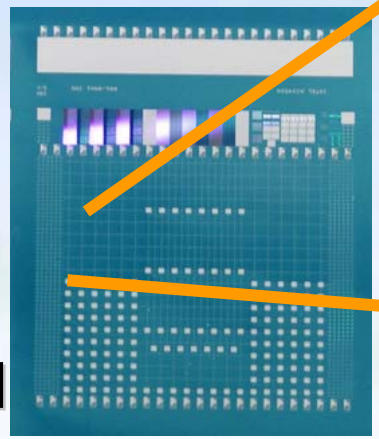
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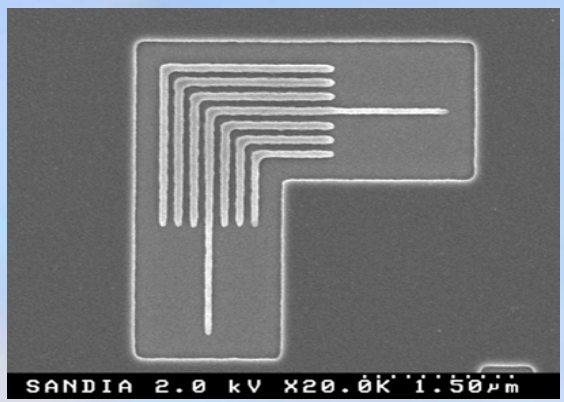
Full Field Images Produced by EUV Prototype Exposure Tool



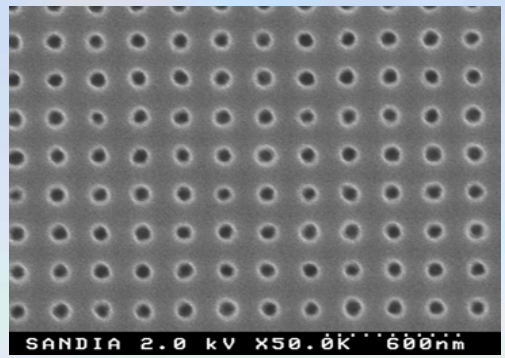
200mm wafer



24 x 32.5mm^2 field



80nm elbows 1:1



100nm contacts 1:1

Commercial EUVL exposure tool feasibility demonstrated

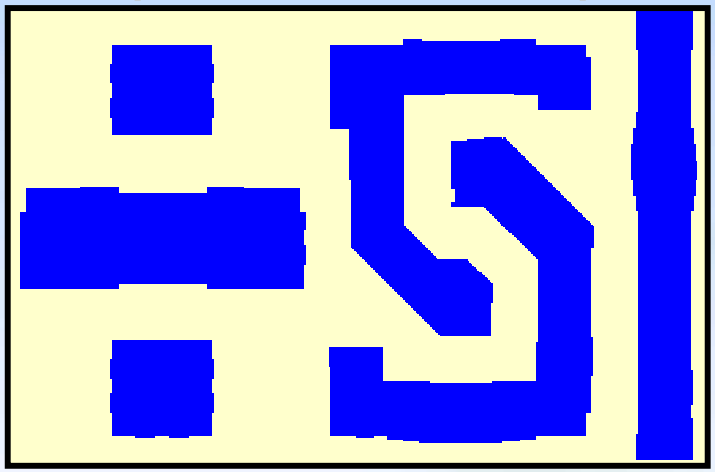
Source: Sandia

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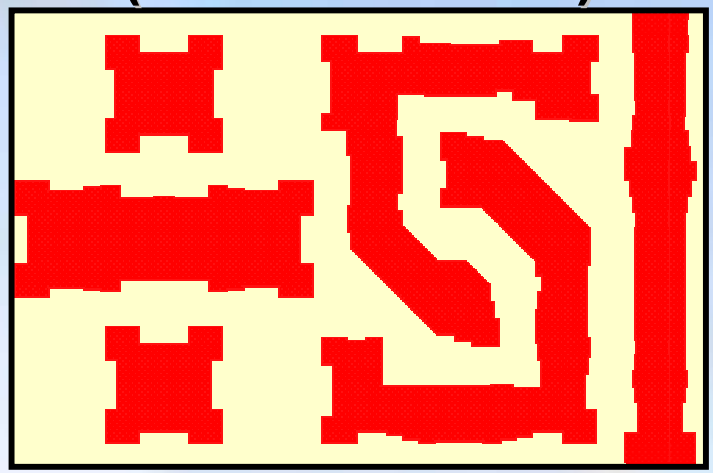
EUV Masks Simpler to Pattern and Inspect than Optical Masks

EUV Mask
(45nm Process)



Est. Cost/Layer:
< $90K

Optical Mask
(45nm Process)



Est. Cost/layer:
$100K (OPC Only)
$150K (OPC + Comp)

EUVL masks will cost less than optical lithography masks

EUVL Being Developed and Commercialized Worldwide

Japan

> 10 Companies

Consortia:

- ASET
- EUVA
- MIRAI



Europe

> 50 Companies

Consortia:

- PREUVE
- MEDEA+
- LETI
- IMEC

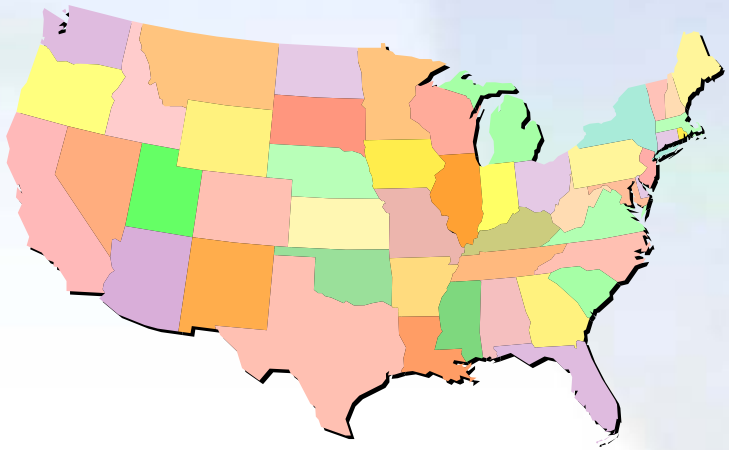


US

> 40 Companies

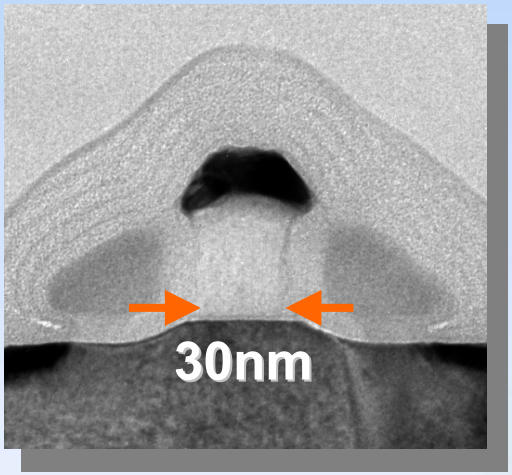
Consortia:

- EUV LLC
- I-SEMATECH
- VNL RDC
- SRC

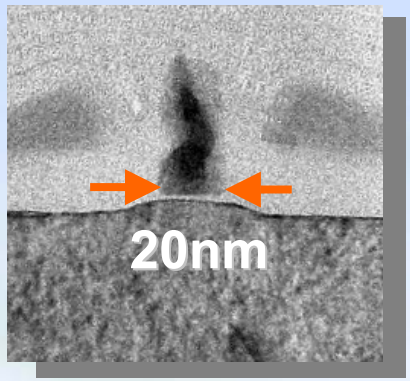


Intel's Transistor Research in Deep Nanotechnology Space

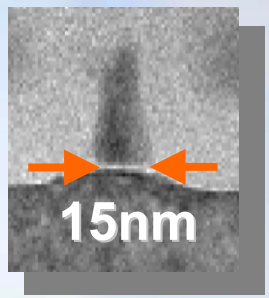
Experimental transistors for future process generations



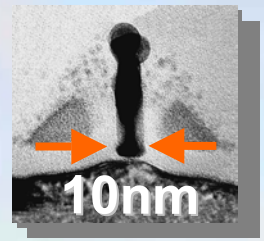
65nm process
2005 production



45nm process
2007 production



32nm process
2009 production



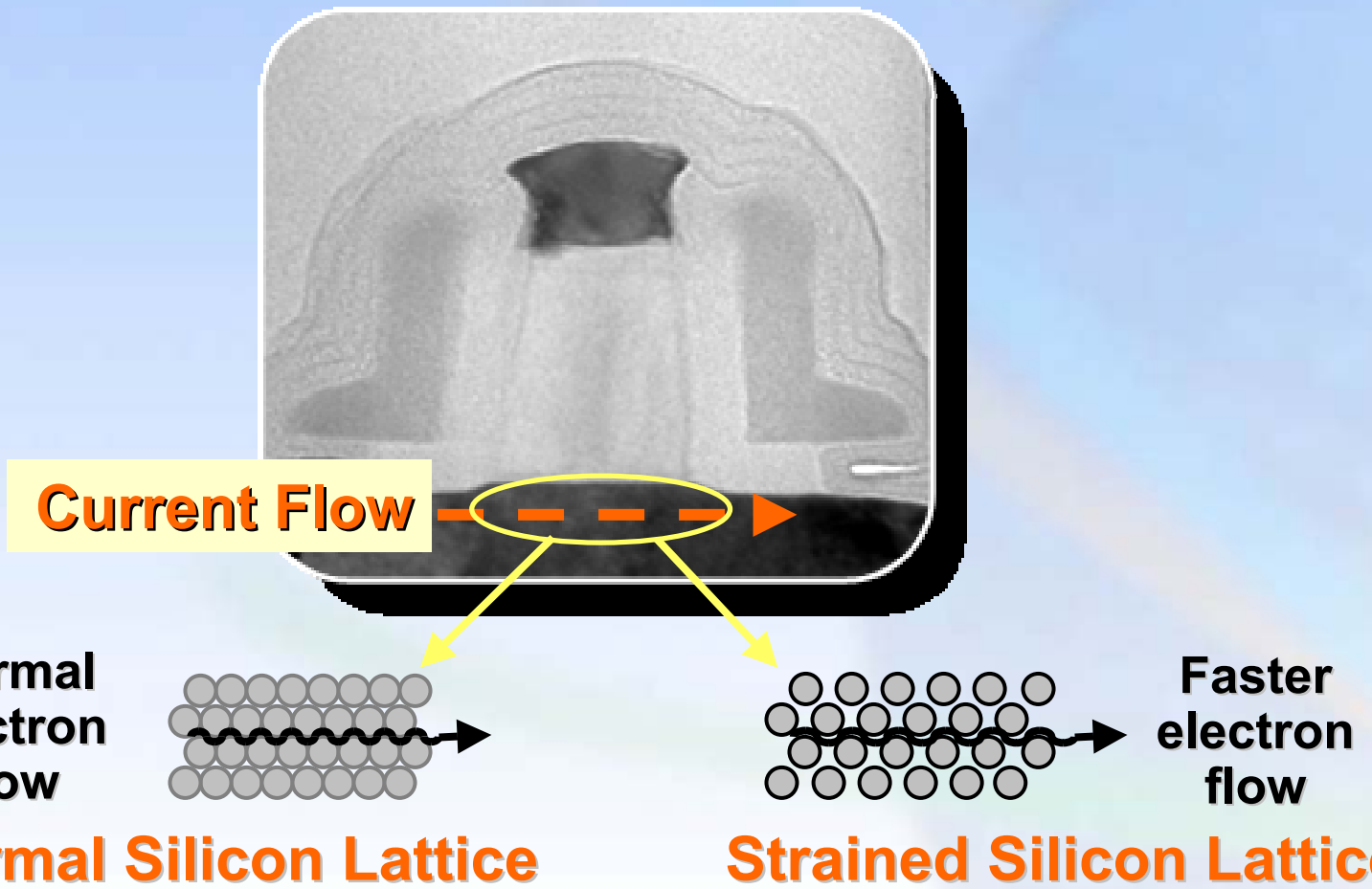
22nm process
2011 production

Transistors will be improved for production

Source: Intel

intel
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Intel's Transistors Run Fast on 90nm Strained Silicon Process



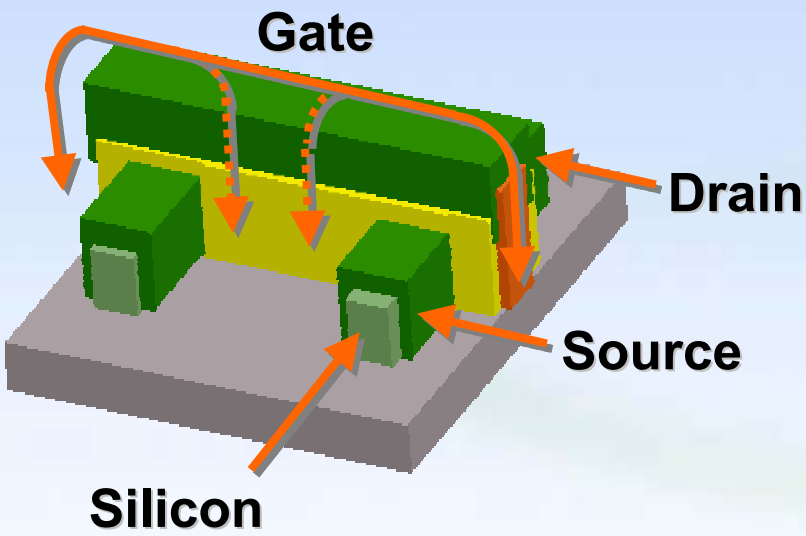
A new way to speed up with nanotechnology

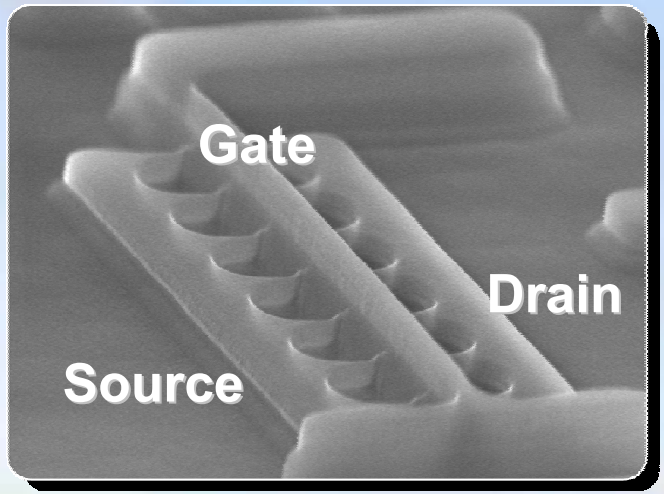
Source: Intel

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Transistors Improved by Going 3-D

Intel's experimental Tri-gate transistor raises performance, lowers off current





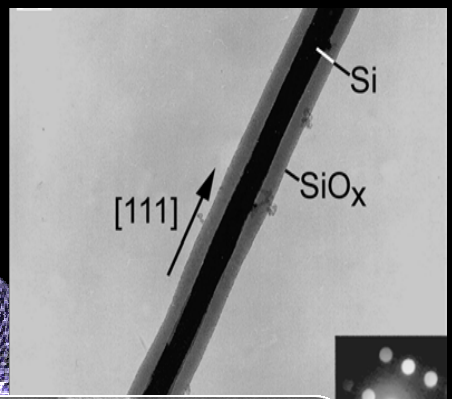
New nanotechnology device options coming

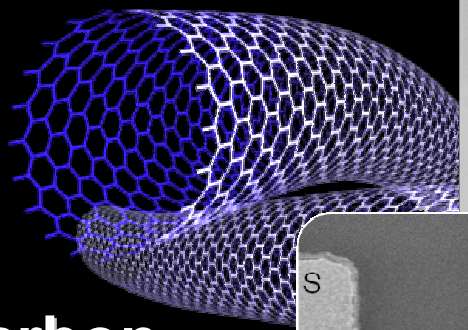
Source: Intel

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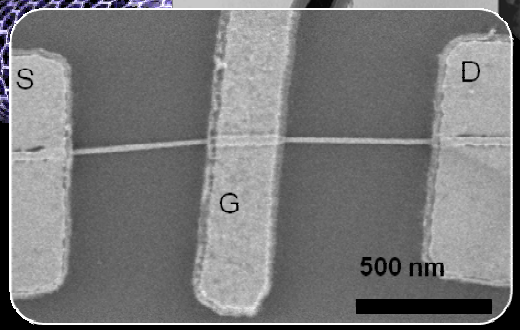
Future Nanotechnology will Ride on Silicon Technology Base

Silicon Nanowire*





Carbon Nanotube



Nanotube/Nanowire Transistors

Molecular Electronics Nanodevices



Innovations expected to overcome scaling limits

*Source: Morales & Lieber, Harvard Univ

Nanotechnology Brings Welcomed Opportunities

- Renewal and extension of silicon technology
 - New materials, processes and device structures
 - Integrate innovations into silicon technology base
 - Break limits of “static” silicon scaling model
- Intel plans to lead in nanotechnology
 - Already in production with nanotechnology
 - Heavily engaged in nanotechnology R&D
 - Best positioned to use nanotechnology innovations

Video

Nanotechnology extends Silicon Technology

Dr. R. Stanley Williams
HPL Fellow, Director, Quantum Science Research
Hewlett-Packard Labs

Professor Yoshio Nishi
Professor Electrical Engineering
Director, Stanford Nano Fabrication Facility

Silicon Integration for Convergence: Three Strategic Combinations

- Computing + Communications
 - Use silicon scaling and integration to improve performance, energy efficiency, cost
- CMOS Base + Application Specific Modules
 - Shared CMOS base for economy of scale
 - Process modules optimized for each application
- Silicon Technology Base + Nanotechnology
 - Nanotechnology innovations will ride on silicon
 - Intel leading nanotechnology production, R&D



intel